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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,620	10/20/2003	Junichiro Nakayama	914-170	4687

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EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,620	NAKAYAMA, JUNICHIRO	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) 21-28 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04/01/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

1. Applicant's election without traverse of claims 1-20 in the reply filed on 05/03/05 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teramoto et al. (US publication 2003/0059991) in combination with Yamazaki (US publication 2004/0201874), Fujimura (2005/0148119), Takaoka et al. (US patent 4,584,025), and Yamanaka (US publication 2003/0148565).

With respect to claims 1, 2, 3, and 7, Teramoto et al. teach a method for manufacturing a semiconductor device comprising (see all disclosed figures and associated text, specifically fig. 12A and claims 17-19 and [0120]):

1) forming a semiconductor material layer 603 on a substrate 601;

2) irradiating at least a region of the semiconductor material layer with a laser for heating and melting the semiconductor material layer in the region; and

3) heating the semiconductor material layer to a temperature in a range of 500 C or higher or crystallization temperature (450-750 C) of the semiconductor layer.

Further with respect to claims 1, 2, 3, and 7, since Teramoto et al. teach the claimed proces that is irradiating the semiconductor material layer and subsequently heating the layer to a crystallization temperature of the semiconductor material layer, uniform cooling of the semiconductor material would inherently be promoted and a polysilicon microstructure would inherently be formed in the semiconductor material layer by lateral solidification from a boundary of the region.

Further with respect to claims 3 and 12, Teramoto et al. teach providing a high thermal conductivity material or silicon nitride layer in proximity to the semiconductor material layer. See [0033]. Note that the presence of high thermal conductivity material or silicon nitride layer in proximity to the semiconductor material layer in Teramoto et al. reference would inherently spread heat in the region and promote uniform cooling in the region.

With respect to claim 4, Teramoto et al. further teach the semiconductor material layer is a silicon film. [0018].

With respect to claim 5, Teramoto et al. further teach directing a laser beam through a mask slit and onto the semiconductor material layer. See [0241].

With respect to claim 6, Teramoto et al. further teach that laser is laser beam or extended laser.

With respect to claims 8 and 9, Teramoto et al. fail to teach the heating for crystallizing the semiconductor material layer is done by laser having wavelength of visible region.

Yamazaki teaches using laser having wavelength of visible region to crystallize semiconductor material layer. See [0023].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Yamazaki into the process of Teramoto et al. to obtain crystallization of the semiconductor material layer. See [0023].

With respect to claim 10, Teramoto et al. further teach forming a high thermal conductivity material layer between the semiconductor material layer and the substrate. See [0033].

With respect to claim 11, Teramoto et al. fail to teach forming a low thermal conductivity material or silicon oxide layer between the high thermal conductivity material and the semiconductor material layer.

Fujimura teaches forming a low thermal conductivity material or silicon oxide layer between a high thermal conductivity material or silicon nitride and a semiconductor material layer to be crystallized. See [0028].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Fujimura into the process of Teramoto et al. to increase yield. See [0006].

With respect to claim 13, the range for the thermal conductivity of the high thermal conductivity material can be determined through routine experimentation and optimization.

With respect to claim 14, Teramoto et al fail to teach forming a cap layer having a thickness on the semiconductor material layer to prevent the unwanted reflection of laser beam.

Takaoka et al. teach forming a cap layer having a thickness on a semiconductor material layer to be crystallized. See col. 3, line 65 to col. 4, line 10.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Takaoka et al. into the process of Teramoto et al. to reduce the reflection of laser beam during crystallization to improve efficiency. See col. 3, line 65 to col. 4, line 10.

With respect to claims 15, 16, 17, and 18, Teramoto et al. fail to teach the applying a magnetic field produced by a magnet perpendicular to the surface of the semiconductor layer during the crystallization or irradiation.

Yamanaka teaches applying a magnetic field produced by a magnet perpendicular to the surface of a semiconductor layer during the crystallization or irradiation. See [0184], [0185] and [0190].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Yamanaka into the process of Teramoto et al. to orient the crystal grains. See [0184], [0185] and [0190].

Further with respect to claim 16, the application of magnetic field would inherently create an electromotive force and movement of melted silicon and would inherently lengthen and widen lateral growth crystals in the resulting polysilicon.

With respect to claim 19, the crystallization of semiconductor material by multiple irradiation is well-known.

With respect to claim 20, since the combined references teach the claimed process, the grain size of resulting polysilicon would be uniformly increased in length and width.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP